CLAIMS

1. Protocol processor intended to be associated with at least one main processor of a system with a view to the execution of tasks to which the main processor is not suited, characterised in that it comprises a program part (30) including an incrementation register (31), a program memory (33) connected to the incrementation register (31) in order to receive addresses thereof, a decoding part (35) intended to receive instructions from the program memory (33) of the program part (30) with a view to executing the said instruction in two cycles, and a data part (36) for executing the instruction.

2. Protocol processor according to Claim 1, characterised in that the decoding part (35) comprises a decoder (37) intended, in each cycle, to generate the address of a register used in the instruction and/or a RAM memory address, the decoder (37) also providing the function of monitoring device receiving interrupt signals and test and set-up signals (TAS) intended for synchronising the system.

3. Protocol processor according to one of Claims 1 and 2, characterised in that the data part (36) consists of a bank of registers (40) connected to multiplexers A and B (41, 42) which are intended to select the various registers or the RAM memories at the input of an arithmetic and logic unit (43), one operation defined in the field of an instruction being executed between two values at the inputs of the arithmetic and logic and shift unit (43) and the result of this operation being carried within the same cycle to the intended address contained in a memory (44) common to the protocol processor and to a main processing unit (45) with which it is associated.

4. Protocol processor according to one of Claims 1 to 3, characterised in that an instruction set composed of at least one field of execution conditions (Figure 10) which is intended therefor comprises three classes of instructions:

- integers corresponding to arithmetic and logic operations on integer numbers,

- transfer corresponding to the transfer operations between register and memory,

- monitoring, corresponding to the monitoring of all the operations modifying the value of the incrementation register (31).

5. Protocol processor according to one of Claims 3 and 4, characterised in that it further comprises a condition monitoring block (60) connected up between the monitoring and decoding device (37) and the stack of registers (40), the condition monitoring block (60) receiving information from the register SW (40d) of the stack of registers (40) and from the condition field of an instruction to be executed.

add B2

Add C2